AMENDMENTS TO THE SPECIFICATION

(1) Please replace the second and third paragraphs (lines 6-10) of the BRIEF DESCRIPTION OF THE DRAWINGS section (page 5) with the following amended paragraphs:

Fig. 2 is a simplified block diagram of a typical graphical adapter [[VGA]] for the generation of text images on a video display in accordance with one embodiment of the present invention.

Fig. 3 is a more detailed schematic diagram of a typical VGA in accordance with one embodiment of the present invention ~~video display controller from the block diagram of the VGA depicted in Fig. 2~~.

(2) Please replace the second paragraph (lines 8-15) on page 6 and the following paragraph (page 6, line 17 to page 7, line 3) with the following amended paragraphs:

Fig. 2 is a block diagram illustrating the general structure of a graphics adapter 14 in accordance with one embodiment of the present invention. The main part of a graphics adapter 14 is the video controller or graphics control chip CRTC (cathode ray tube controller) 16. The CRTC 16 supervises the functions of the adapter 14 and generates the necessary control signal. The CPU 18 accesses the video RAM 20 via the bus interface 22 to write information that defines the text or graphics the monitor 24 is to display. The

CRTC 16 continuously generates addresses for the video RAM 20 to read the corresponding characters, and to transfer them to the character generator 26.

Referring now to Fig. 3, a diagram of a typical VGA in accordance with one embodiment of the present invention ~~CRTC 16~~ is illustrated. In text mode, the characters are usually defined by their ASCII codes, which are further assigned an attribute. The attribute defines the display mode for a particular character more precisely. Some typical attributes include whether it is to be displayed in a blinking, bold, or inverted manner. The character generator RAM, for every ASCII code, holds a pixel pattern for the corresponding character. The character generator 32 converts the character codes using the pixel pattern in the character RAM 30 into a sequence of pixel bits, and transfers them to a shift register 34. The signal generator 36 generates the necessary signals for the monitor 38, using the bit stream from the shift register 34, the attribute information from the video RAM 40, and the synchronization signals from the CRTC 42. The monitor 38 processes the passed video signals and displays the symbolic information in the video RAM 40 in the usual form as a picture.

(3) Please replace the first full paragraph (lines 4-11) on page 9 with the following amended paragraph:

In accordance with another embodiment of the present invention, each lookup table used for generating expanded cell lines is located in VGA memory layer three. Figure 6 illustrates a typical VGA Video RAM 40 organization. VGA Video RAM 40 is organized into four 64K parallel memory layers 70. The character code data for 256

characters resides in memory layer zero 72. The attribute data resides in memory layer one 74. The character generator stores the character definition table for converting the character code into pixel patterns in memory layer two 76. Those of ordinary skill in the art will recognize that memory layer three 78 is normally unused [[78]]. Therefore, the use of memory layer three 78 for the lookup table will not conflict with other uses of the memory.